Development of 5 kW, 1 MHz Solid State RF Pulsed Power Amplifier Using Parallel Configuration of Four LDMOS Transistor at Device and Operated in Single Ended Mode

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Abstract. A 5 kW and 1 MHz pulsed solid-state RF amplifier has been designed and developed to drive TH581 tetrode tube-based RF amplifier to realize 100 kW pulsed RF source. The driver amplifier is operated with a 1 ms pulse width at a 50 Hz repetition rate. The 5 kW RF power is obtained by operating four Gemini pair LDMOS transistors (VDD=50V) in parallel configuration at the device itself and having single-ended topology with common lumped element based input and output matching network. The amplifier delivers 5 kW RF power when fed by 25 dBm RF input drive from the signal generator. This scheme eliminates the need for RF combiner and divider which results in low loss, high efficiency, lesser number of components, simple and compact design. The measured saturated drain efficiency of the power amplifier is around 62%.

Keywords: Solid state RF power amplifier, parallel configuration, LDMOS, ISNS

1. Introduction

A 1 GeV, 1 MW average power, pulsed proton accelerator is being designed for the proposed Indian Spallation Neutron Source (ISNS) at RRCAT, Indore. The 1 GeV, 1-2 ms long proton beam repeating at 50 Hz from the linac will be injected into the accumulator ring [1]. The RF system in the accumulator ring needs to establish 40 kV gap voltage across a ferrite loaded coaxial λ/2 cavity at 1 MHz RF frequency. For this, a prototype linear RF source of 100 kW pulse power rating at 1 MHz having maximum duty cycle 10% and pulse repetition rate of 50 Hz is to be developed [2-3]. This 100 kW pulsed power amplifier will require driver amplifier of around 5 kW pulse power rating at 1 MHz. The Laterally diffused MOSFET device (LDMOS)[4] which is now available up to power rating of 1.5 kW from many manufacturer is obvious choice for the driver amplifier. These solid-state device exhibits important advantages over vacuum tubes including higher reliability and longer life, small size and weight, lower cost and easier cooling. Generally, divide and combine topology [6-9] is used to develop a linear power amplifier delivering larger output power levels than that is achievable from single active devices. This topology has losses due to finite insertion loss, return loss and isolation of RF combiner. Moreover, phase and amplitude imbalance within different amplifier modules are also needed to be minimized suitably. Another topology, mostly used at low frequencies to get high power uses switched-mode tuned power amplifiers in which active devices is assumed to be ideally driven in the ON and OFF states. This topology is considered as a DC-to-RF power converter rather than an amplifier [10] and it exhibits highly nonlinear behavior.

In order to develop a solid-state driver amplifier of 5 kW pulsed power rating using LDMOS, multiple (four) LDMOS have been paralleled in single-ended configuration and operated in linear mode. Four LDMOS, each having 1.25 kW power rating, are placed symmetrically to excite common input and output matching networks. Functionally this adds the four in-phase voltage-controlled current sources in common output matching network and generates ~ 5 kW (4×1.25 kW) RF output power. To swamp out the variation in the input impedance of four LDMOS devices and to damp spurious oscillations, the common input has been loaded directly by 50 ?. Using this scheme, the need of RF combiner and divider are eliminated which results in low loss, high efficiency, lesser number of components, simple and compact design.

This paper presents design, realization and test results of 5 kW, 1 MHz pulsed solid-state RF amplifier developed using a parallel configuration of four LDMOS in single-ended mode.

2. Design description

The application needs a bandwidth of less than a percent (±10 kHz) which permits the use of narrowband amplifier design. The NXP make MRFE6VP61K25HR6 which is unmatched input and output LDMOS transistors is selected for the design of amplifier at 1 MHz. Since impedance representing test circuit impedance as measured from gate to gate (Z_{source}) and measured from drain to drain (Z_{load}) in balanced configuration has been provided in the datasheet from 1.8 MHz onwards for 1.25 kW peak power in class AB mode, the same is not given at 1 MHz.The optimum large-signal load resistance to deliver *Po* RF power in single-ended mode has been calculated by the following equation

$$R_L = ((V_{DD}{}^2)/(2 \times P_o)) \quad (1)$$

Where V_{DD} is drain voltage. Equation (1) is derived considering the output tuned circuit as a high Q parallel resonant circuit or an equivalent network and neglecting drain source on voltage. A low-pass Π output matching network is chosen and designed which transforms 50 Ω dummy load to R_L at 1 MHz. The Q factor of the matching network circuit was decided in such a way that it yields required harmonic attenuation(-30 dB) and bandwidth. The

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component values of the output matching network were calculated accordingly. For the available Q factor of the matching network components, total circuit component power loss in output matching network was estimated to be less than 10% of P_O by assuming a purely sinusoidal voltage of amplitude V_{DD} at the drain. The input matching network is parallel resonant circuit having a shunt dummy resistor (50 Ω), a shunt inductor and total input capacitance which also takes into account of miller capacitance at input due to gate drain capacitance. Common gate bias is applied through a resistive feed having value around 40 times of dummy resistor (50 Ω), so that it has negligible effect on the input matching network. The drain voltage is applied through NiZn ferrite core based radio frequency choke (RFC) of Fair-rite having range of inductive applications up to 25 MHz. The reactance of RFC is also around 40 times of R_L at 1 MHz. The other end of RFC has been made RF ground with the help of ATC make bypass capacitor so that RF voltage going in to the DC power supplies is negligible. The magnitude of average current required to produce P_O CW RF power is supplied by electrolytic capacitor placed across 50 V drain power supply during RF pulse on. The total quiescent current I_{DQ} of around 800 mA was set using potentiometer. In order to measure pulsed dc current drawn by power amplifier from electrolytic capacitor at drain during RF pulse on, a closed loop non-contacting type hall effect based LEM current transducer has been utilised having -1 dB frequency bandwidth ≤ 200 kHz. All the components are assembled on FR4 dielectric based PCB. The four LDMOS has been mounted directly on air cooled heat sink measuring 300 mm by 270 mm. RF intensity measurement was done close to the power amplifier and maximum RF leakage was found to be 2 mW/cm^2 near L2 inductor of output matching network which is much less than the permitted limit (100 mW/cm^2 at 1 MHz). The complete circuit schematic of the RF amplifier is shown below with common input matching network, common output matching network, gate and drain bias circuit.

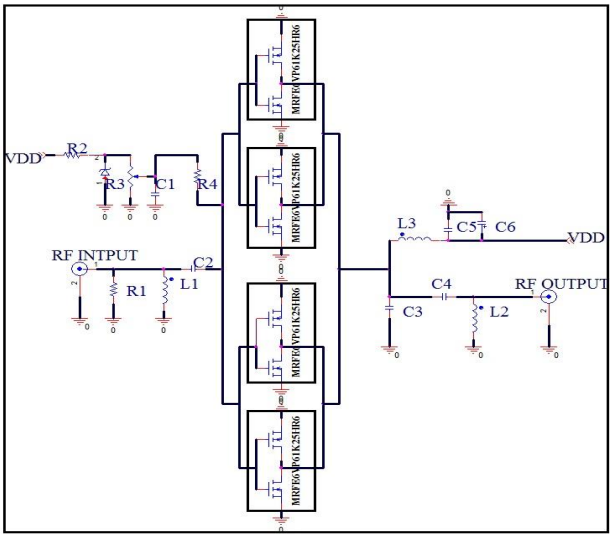

Fig. 1. Complete circuit schematic of 5 kW pulsed RF Amplifier at 1 MHz

2.1. Circuit schematic of the amplifier

In Figure 1, component R1(50 Ω), L1,C2 and total input gate to source capacitance forms the input matching network. The capacitor C2 in the input matching network is RF coupling capacitor which acts as a short at 1 MHz. The capacitor C3, C4 and inductor L2 constitute output matching network.The resistor R2, R3 and R4(resistive feed), 3.3 V Zener diode, and capacitor C1 forms gate bias circuit. The drain RFC L3, C5 and electrolytic capacitor C6 is part of drain bias circuit.

2.2. Input matching network

Since the value of input capacitance (C_{iss}), reverse transfer capacitance (C_{rss}), and forward transconductance (g_{fs})is available in the datasheet at 1 MHz, the value of input gate to source capacitance when four LDMOS in the schematic are paralleled comes out to be eight times the gate source capacitance (C_{gs}) of single transistor as each MRFE6VP61K25HR6 contains two dies in the same package. The input miller capacitance due to gate drain capacitance (C_{gd}) was also then calculated and found to be $(8 \times C_{gd}) \times (1 - A_V)$ where $A_V = (-8 \times g_{fs} \times Z'_L)$ is small signal voltage gain taking low frequency assumption and neglecting admittance between gate to drain (Y_{gd}) and admittance between drain to source (Y_{ds}) at 1 MHz. The Z'_L is parallel combination of $(r_d/8)$ (r_d=drain resistance) and R_L (load resistance presented to common drain by output matching network at 1 MHz) which effectively comes out to be R_L. The total input capacitance at 1 MHz was roughly estimated by the equation

$$C_i = (8 \times C_{gs} + (8 \times C_{gd}) \times (1 - A_V)) \quad (2)$$

This total input capacitance C_i was then tuned out by a shunt inductor L1 having value given by equation

$$L1 = 1/\omega^2 C_i \quad (3)$$

where ω is 2Πf and f is 1 MHz. A 50 Ω dummy shunt resistor R1 matches the input of the amplifier to RF input signal source at 1 MHz.

Figure 3 shows the simulated impedance response of input matching network on smith chart which is around 50 Ω at 1 MHz. Figure 4 is the input impedance response of the amplifier measured by R&S make two-port VNA keeping bias supply (gate and drain) on which is also found to be very near to 50 Ω at 1 MHz.

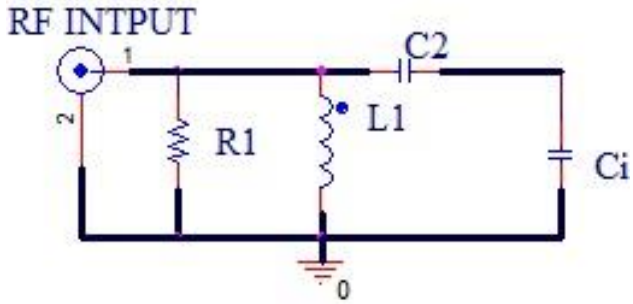

Fig. 2. Input matching network of the amplifier where C2 is RF coupling capacitor

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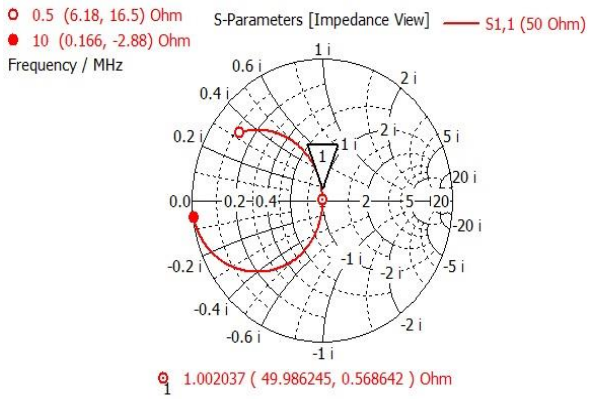


Fig. 3. The simulated response of input matching network vs frequency

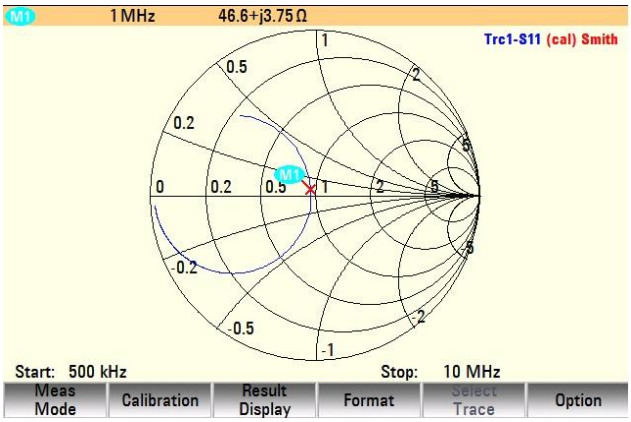
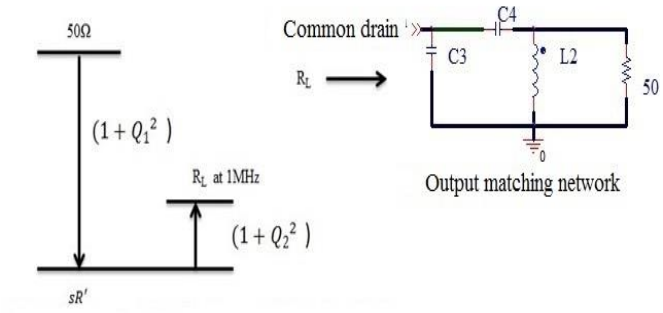


Fig. 4. The measured response of input impedance of RF power amplifier with drain and gate bias supply on

2.3. Output matching network



Steps of impedance transformation at output

$Q_1 = 18.2, R' = 50/(1+Q_1^2)$

$Q_2 = 0.6, Q_2 = ((R_L/R') - 1))^{0.5}$

$R_L = V_{DD}^2/(2 \times P_O)$

$V_{DD} = 50\,V, P_O = 6000\,W$

Fig. 5. Downward transformation of the 50 Ω output dummy load to optimum load resistance RL using low pass Π section needed to generate 6 kW peak power at 1 MHz

The value of R_L was calculated using Eq.(1) taking output power P_O = 6 kW and V_{DD}=50 V since RF power loss in the components of output matching network is estimated to be around 10% of P_O due to finite Q factor of its components and we need 5 kW useful output power. The value of R_L comes out to be 0.21 Ω. A Π output matching network topology transforms 50 Ω dummy load to optimum value of R_L (0.21 Ω) at f =1 MHz. It also presents nearly short impedance at harmonics frequency so that harmonic content in the output signal is below -30 dBc. The downward transformation of impedance has been done by two associated transformation Q factor (Q_1 and Q_2). The first transformation Q (Q_1) transforms parallel equivalent of 50 Ω and L2 to series equivalent R'(Lower than R_L) and a reactive part. The second transformation Q (Q_2) transforms R' to R_L at 1 MHz. The value of capacitance between common drain and source with four LDMOS paralleled also comes out to be eight times of drain to source capacitance (C_{ds}) of single transistor. This value of drain to source capacitance and miller output capacitance due to C_{gd} becomes part of output matching network capacitor C3 so that common drain sees a purely resistive load of R_L at 1 MHz . ATC make capacitor having Q factor ≥ 600 at 1 MHz and working voltage 2 kV is selected for C4 . This capacitor is made of NPO grade ceramic having temperature coefficient of capacitance ±30 ppm .The X7R ceramic based ATC capacitor has been used for C3 which has Q factor ≥ 50 at 1 MHz. The Q factor of inductor L2 is measured with Wayne Kerr make impedance analyser which is around 650 at 1 MHz and its self-resonant frequency is more than 10 MHz. This topology of output matching network eliminates the need of DC blocking capacitor at the drain of the amplifier as capacitor C4 of output matching network also serves for the same purpose. Figure 6 shows the simulated impedance response of output matching network which is 0.21 Ω (purely resistive) at 1 MHz.

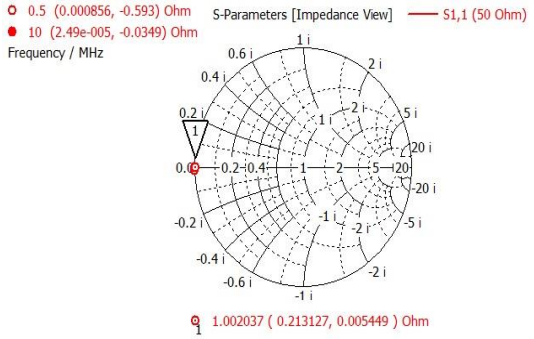


Fig. 6. The simulated impedance response of output matching network at common drain vs. frequency

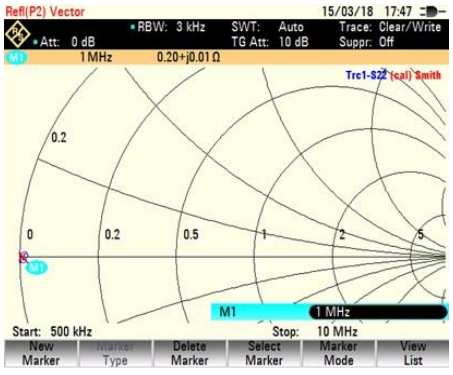


Fig.7. The measured impedance response of output matching network at common drain @1 MHz with LDMOS not soldered

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Figure 7 shows the measured impedance response of assembled matching network with VNA without soldering LDMOS which is around 0.20 Ω(resistive) at 1 MHz.

3. Test results of power amplifier

Table1. Amplifier Specifications and Performance.

Sr. No.	Parameter	Value
1	Maximum RF power output/ nominal power gain	5 kW/42 dB
2	Operating frequency and 1 dB bandwidth	1 MHz, ±20 kHz
3	Operating mode/ class of operation	Pulsed/AB
4	Saturated efficiency	62%
5	Pulse width/duty cycle(%)	1 ms/5%
6	1 dB compression point	67 dBm
7	Harmonic distortion	-30 dBc
8	Cooling	Forced air cooled

Table 1 presents the various RF parameters of developed 5 kW, 1 MHz pulsed RF amplifier. Figure 8 is the photograph of developed RF amplifier showing all its components. Figure 9 is the plot of output power vs. power gain (dB) and drain efficiency(%). It shows that maximum power gain and efficiency is around 42 dB and 62% at 0061 round 5 kW RF power. Figure 10 is the transfer curve (input vs output) at three different frequency. Figure 11 is the plot of output power vs. frequency keeping the input drive same. Figure 12 is the FFT of output waveform at around 4.5 kW pulse power indicating that amplitude of harmonic components at 2 MHz, 3 MHz, 4 MHz etc. are around -30 dB down in comparision to fundamental component at 1 MHz. Figure 13 is measurement of current supplied by capacitor charging power supply at drain to amplifier operating at 5 kW peak power which is around 20×7.8 A during RF pulse on. Figure 3 shows a comparison of measured and simulated VSWR curves of the proposed antenna. From this figure, it can observe that the measured VWSR is in good agreement with the simulated one. The antenna rejects the bandwidth of WiMAX and WLAN which covers the frequency range from 2.89 to more than 14 GHz for VSWR ≤ 2 covering the entire UWB (3.1-10.6 GHz) frequency band. Hence, this antenna rejects the interference of WiMAX (3.3-3.7 GHz) and WLAN (5.725-5.825 GHz) bands.

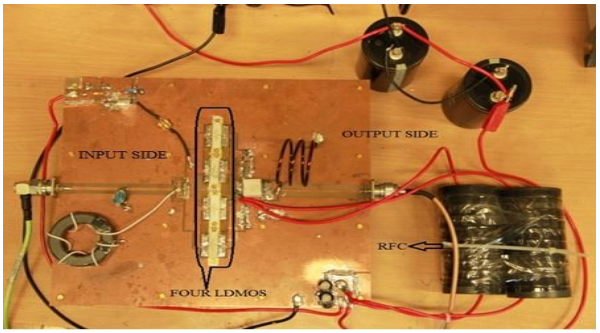

Fig. 8. Photograph of 5 kW pulsed amplifier module

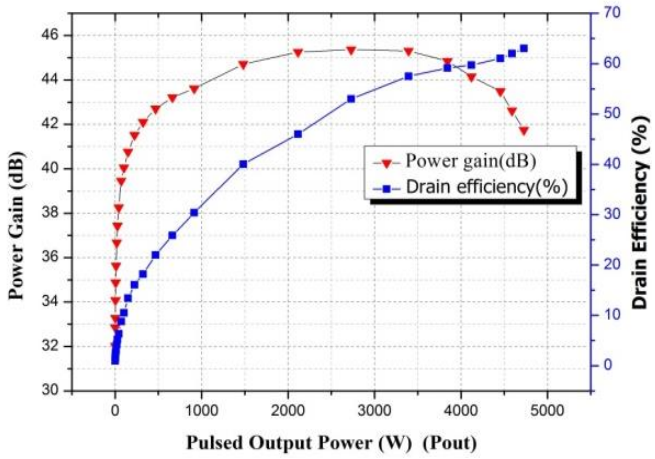

Fig. 9. Measured power gain and drain efficiency vs. output power of 5 kW power amplifier

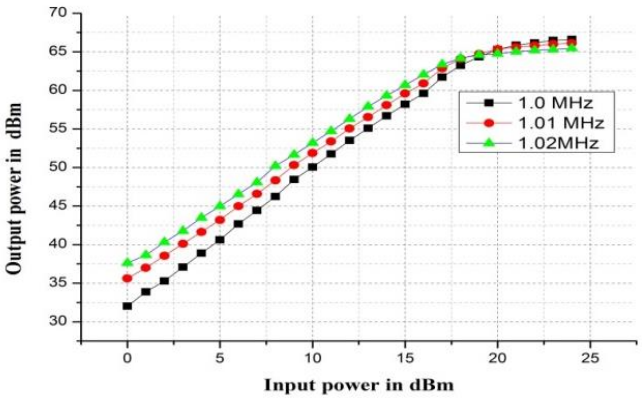

Fig. 10. Measured output power vs. input power of RF power amplifier

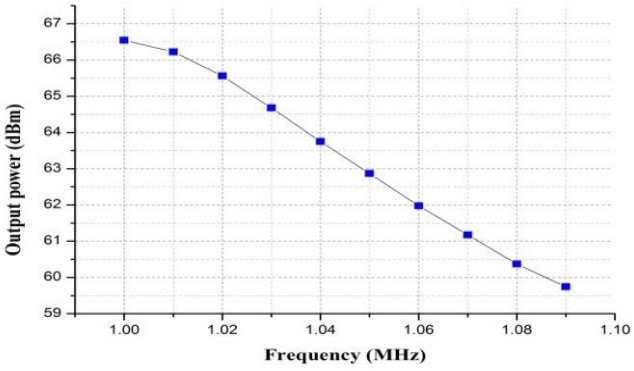

Fig.11. RF power vs. frequency

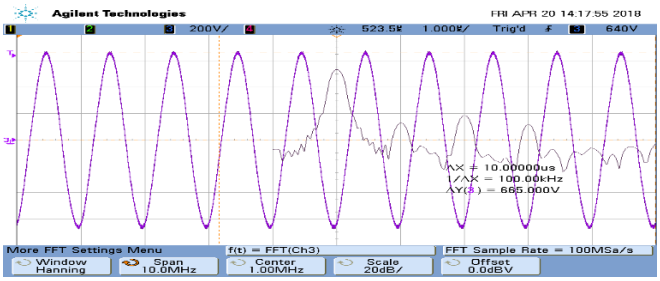

Fig. 12. FFT of output signal at around 4.5 kW pulsed RF power

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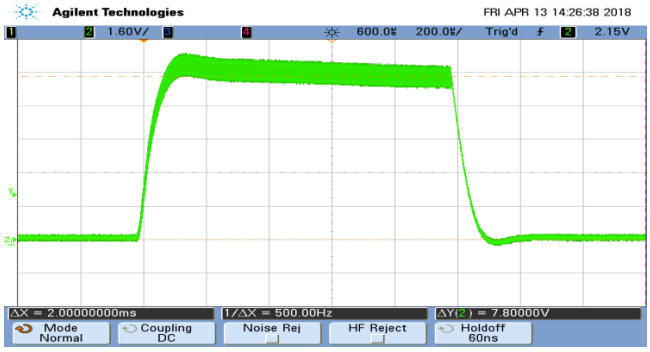

Fig. 13. Measured pulsed current waveform which is supplied to amplifier by capacitor charging power supply at drain during RF pulse on . 1 V of the scale indicates 20 A of pulse current. The sensor used to measure current is based on through line Hall effect of LEM make

4. Conclusion

A compact 5 kW linear RF pulsed power amplifier has been successfully designed and developed at 1 MHz by direct paralleling of four LDMOS transistors at device level. The driver amplifier delivers 5 kW RF power at 1 MHz when driven directly by a local oscillator having maximum drive of 25 dBm without any instability. This amplifier has successfully replaced the earlier developed tetrode tube TH561 based driver amplifier for 100 kW pulsed final amplifier using TH581 tetrode tube. With this driver amplifier, the final tetrode amplifier has been tested up to 100 kW pulsed power satisfactorily. This has resulted in compact complete amplifier system and reduced complexity.

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Rajendra Kumar Deo completed his B.E. in Electronics and communication from Vinoba Bhave University, Hazaribagh in the year 1999. He joined RRCAT, Indore in 2001 as a scientific officer. Since then he has worked for commisioning of 4 no. of 64 kW CW klystron based RF power amplifier for Indus-2 at the operating frequency 505.816 MHz. He has also worked for commisioning of 10 kW pulsed planar triode based RF power amplifier for IR-FEL at the operating frequency 476 MHz. He is also working for development of 100 kW tetrode tube based RF power amplifier for Accumulator ring in ISNS at the operating frequency 1 MHz.

M.K. Jain completed his B.E. in Electronics from University of Rajsthan , Jaipur in the year 1988. He joined RRCAT, Indore in 1990 as a scientific officer. His area of work is high power tube based RF amplifier, power combiners, directional couplers, and high-power rigid line components.

Mahendra Lad completed his B.E. in (Electronics and Telecommunication) from Devi Ahilya University, Indore in 1986. He joined RRCAT in 1987 as a scientific officer. Since then he is involved in RF system development for Indus-1 and Indus-2 Synchrotron Radiation Sources at the centre.